Sol P. DiJaili et al.

Applicant: Serial No.:

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Att'y Docket No.: 15436.247.40.1.1

Confirmation No.: 7346

Group: 2633

Sheet 1 of 7

OPTICAL LATCH BASED ON LASING SEMICONDUCTOR OPTICAL AMPLIFIERS



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Form PTO-1449 Sheet 6 of 7 Confirmation No.: 7346 Applicant: Sol P. DiJaili et al. Serial No.: 10/789,126 Att'y Docket No.: 15436.247.40.1.1 February 27, 2004 Filing Date: Group: 2633 OPTICAL LATCH BASED ON LASING SEMICONDUCTOR OPTICAL AMPLIFIERS For: F. Koyama et al., Multiple-Quantum-Well GalnAs/GalnAsP Tapered Broad-Area Amplifiers with Monolithically Integrated Waveguide Lens for High-Power Applications, IEEE Photonics Technology Letters, Vol. 5, No. 8, pp. 916-919, August 1993. 75 J.C. Simon et al., Travelling Wave Semiconductor Optical Amplifier with Reduced Nonlinear Distortions, Electronics Letters, Vol. 30, No. 1, pp. 49-50, January 6, 1994. - 76 L.F. Tiemeijer et al., 1310-nm DBR-Type MQW Gain-Clamped Semiconductor Optical Amplifiers with AM-CATV-Grade Linearity, IEEE Photonics Technology Letters, Vol. 8, No. 11, pp. 1453-1455, November 1996. L.F. Tiemeijer et al., High-Gain 1310 nm Semiconductor Optical Amplifier Modules with a R____ 77 Built-in Amplified Signal Monitor for Optical Gain Control, IEEE Photonics Technology Letters, Vol. 9, No. 3, pp. 309-311, March 1997. **—** 78 Agility Unveils Long-Haul Laser, Light-Reading - The Global Site for Optical Networking, retrieved from internet www.lightreading.com/document.asp, March 30, 2001. Wolfson et al., Detailed Theoretical Investigation of the Input Power Dynamic Range for Gain-Clamped Semiconductor Optical Amplifier Gates at 10 Gb/s, IEEE Photonics Technology Letters, 1998, Vol. 10, No. 9, pp. 1241-1243. 80 F. Robert et al., All-Optical Set-Rest Operation of a Bistable Semiconductor Laser Intracavity-Coupled to a Vertical-Cavity Surface-Emitting Laser, IEEE Photonic Technology, Letters, Vol. 12, No. 5, May 2000, pp. 465-467. \mathbb{Z}_{2} _81 D.B. Shire et al., Gain Controlled Vertical Cavity Surface Emitting Lasers Coupled with Intracavity In-plane Lasers, Appl. Phys. Lett. Vol. 66, No. 14, April 3, 1995, pp. 1717-1719.

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While the filing of Information Disclosure Statements is voluntary, the procedure is governed by the guidelines of Section 609 of the Manual of Patent Examining Procedure and 37 C.F.R. §§ 1.97 and 1.98. To be considered a proper Information Disclosure Statement, Form PTO-1449 shall be accompanied by a copy of each listed patent or publication or other item of information and a translation of the pertinent portions of foreign documents (if an existing translation is readily available to the applicant), an explanation of relevance of each reference not in the English language, and should be submitted in a timely manner as set out in MPEP Sec. 609.

Examiners will consider all citations submitted in conformance with 37 C.F.R. § 1.98 and MPEP Sec. 609 and place their initials adjacent the citations in the spaces provided on this form. Examiners will also initial citations not in conformance with the guidelines which may have been considered. A reference may be considered by the Examiner for any reason whether or not the citation is in full conformance with the guidelines. A line will be drawn through a citation if it is not in conformance with the guidelines AND has not been considered. A copy of the submitted form, as reviewed by the Examiner, will be returned to the applicant with the next communication. The original of the form will be entered into the application file.

Each citation initialed by the Examiner will be printed on the issued patent in the same manner as references cited by the Examiner on Form PTO-892.

The reference designations "A1," "A2," etc. (referring to Applicant's reference 1, Applicant's reference 2, etc.) will be used by the Examiner in the same manner as Examiner's reference designations "A," "B," "C," etc. on Office Action Form PTO-1142.

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